

Claims

- 1 1. A method for forming a structure, the method including:
2 forming a compressively strained semiconductor layer, the compressively strained layer
3 having a strain greater than or equal to 0.25%; and
4 forming a tensilely strained semiconductor layer over the compressively strained layer,
5 wherein the compressively strained layer is substantially planar, having a surface
6 roughness characterized by at least one of (i) an average roughness wavelength greater than an
7 average wavelength of a carrier in the compressively strained layer and (ii) an average roughness
8 height less than 10 nm.
- 1 2. The method of claim 1, wherein the compressively strained layer comprises at least one
2 group IV element.
- 1 3. The method of claim 1, wherein the compressively strained layer comprises at least one
2 of silicon and germanium.
- 1 4. The method of claim 3, wherein the compressively strained layer comprises >1%
2 germanium.
- 1 5. The method of claim 1, wherein the tensilely strained layer comprises silicon.
- 1 6. The method of claim 1, wherein the compressively strained layer comprises at least one
2 of a group III and a group V element.
- 1 7. The method of claim 6, wherein the compressively strained layer comprises indium
2 gallium arsenide.
- 1 8. The method of claim 6, wherein the compressively strained layer comprises indium
2 gallium phosphide.
- 1 9. The method of claim 6, wherein the compressively strained layer comprises gallium
2 arsenide.
- 1 10. The method of claim 1, wherein the compressively strained layer comprises at least one

2 of a group II and a group VI element.

1 11. The method of claim 10, wherein the compressively strained layer comprises zinc
2 selenide.

1 12. The method of claim 10, wherein the compressively strained layer comprises sulphur.

1 13. The method of claim 10, wherein the compressively strained layer comprises cadmium
2 telluride.

1 14. The method of claim 10, wherein the compressively strained layer comprises mercury
2 telluride.

1 15. The method of claim 1, wherein the compressively strained layer has a thickness of less
2 than 500 Å.

1 16. The method of claim 15, wherein the compressively strained layer has a thickness of less
2 than 200 Å.

1 17. The method of claim 1, wherein the compressively strained layer is formed at a first
2 temperature, at least a portion of the tensilely strained layer is formed at a second temperature,
3 and the second temperature is greater than the first temperature.

1 18. The method of claim 17, wherein the tensilely strained layer comprises silicon and the
2 second temperature is greater than 450 °C.

1 19. The method of claim 17, wherein forming the tensilely strained layer at a second
2 temperature includes initially forming a first portion of the tensilely strained layer at the first
3 temperature and forming a second portion of the tensilely strained layer at the second
4 temperature, the first temperature being sufficiently low to substantially avoid disruption of
5 planarity, the first portion of the tensilely strained layer maintaining the planarity of the
6 compressively strained layer notwithstanding transition to the second temperature.

1 20. The method of claim 1, wherein the tensilely strained layer is formed at a rate greater
2 than 100 Å/hour.

- 1 21. The method of claim 1, wherein the compressively strained layer is formed by chemical
2 vapor deposition.
- 1 22. The method of claim 1, wherein the tensilely strained layer is formed by chemical vapor
2 deposition.
- 1 23. The method of claim 1, wherein the wavelength of the surface roughness is greater than
2 10 nanometers.
- 1 24. A structure comprising:
2 a compressively strained semiconductor layer having a strain greater than or equal to
3 0.25%; and
4 a tensilely strained semiconductor layer disposed over the compressively strained layer,
5 wherein the compressively strained layer is substantially planar, having a surface
6 roughness characterized by at least one of (i) an average roughness wavelength greater than an
7 average wavelength of a carrier in the compressively strained layer and (ii) an average roughness
8 height less than 10 nm.
- 1 25. The structure of claim 24, wherein the compressively strained layer comprises a group IV
2 element.
- 1 26. The structure of claim 25, wherein the compressively strained layer comprises at least
2 one of silicon and germanium.
- 1 27. The structure of claim 26, wherein the strain of the compressively strained layer is greater
2 than 1%.
- 1 28. The structure of claim 24, wherein the compressively strained layer has a thickness of
2 less than 500 Å.
- 1 29. The structure of claim 28, wherein the compressively strained layer has a thickness of
2 less than 200 Å.
- 1 30. The structure of claim 24, wherein the wavelength of the surface roughness is greater
2 than 10 nanometers.

- 1 31. The structure of claim 24, wherein the tensilely strained layer comprises silicon.
- 1 32. The structure of claim 24, wherein the compressively strained layer comprises at least
2 one of a group III and a group V element.
- 1 33. The structure of claim 32, wherein the compressively strained layer comprises indium
2 gallium arsenide.
- 1 34. The structure of claim 32, wherein the compressively strained layer comprises indium
2 gallium phosphide.
- 1 35. The structure of claim 32, wherein the compressively strained layer comprises gallium
2 arsenide.
- 1 36. The structure of claim 24, wherein the compressively strained layer comprises at least
2 one of a group II and a group VI element.
- 1 37. The structure of claim 36, wherein the compressively strained layer comprises zinc
2 selenide.
- 1 38. The structure of claim 36, wherein the compressively strained layer comprises sulphur.
- 1 39. The structure of claim 36, wherein the compressively strained layer comprises cadmium
2 telluride.
- 1 40. The structure of claim 36, wherein the compressively strained layer comprises mercury
2 telluride.
- 1 41. The structure of claim 24, further comprising:
2 a first transistor formed over the compressively strained layer, the first transistor
3 including:
4 (i) a first gate dielectric portion disposed over a first portion of the
5 compressively strained layer,
6 (ii) a first gate disposed over the first gate dielectric portion, the first gate
7 comprising a first conducting layer, and

(iii) a first source and a first drain disposed proximate the first gate and extending into the compressively strained layer.

42. The structure of claim 41, wherein the first transistor is an n-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise n-type dopants.

43. The structure of claim 41, wherein the first transistor is a p-type metal-oxide-semiconductor field-effect transistor and the first source and first drain comprise p-type dopants.

44. The structure of claim 41, further comprising:

a second transistor formed over the compressively strained layer, the second transistor including:

(i) a second gate dielectric portion disposed over a second portion of the compressively strained layer,

(ii) a second gate disposed over the second gate dielectric portion, the second gate comprising a second conducting layer, and

(iii) a second source and a second drain disposed proximate the second gate and extending into the compressively strained layer,

wherein the first transistor is an n-type metal-oxide-semiconductor field-effect transistor, the first source and first drain comprise n-type dopants, the second transistor is a p-type metal-oxide-semiconductor field-effect transistor, and the second source and second drain comprise p-type dopants.